

**Client**      **Defense Organization**

**Project**     **High speed ADC.**

### **Requirement**

Design of a High speed 12 bit ADC for capturing high speed data from field and APIs for initiating start/stop from a user system, downloading data from ADC

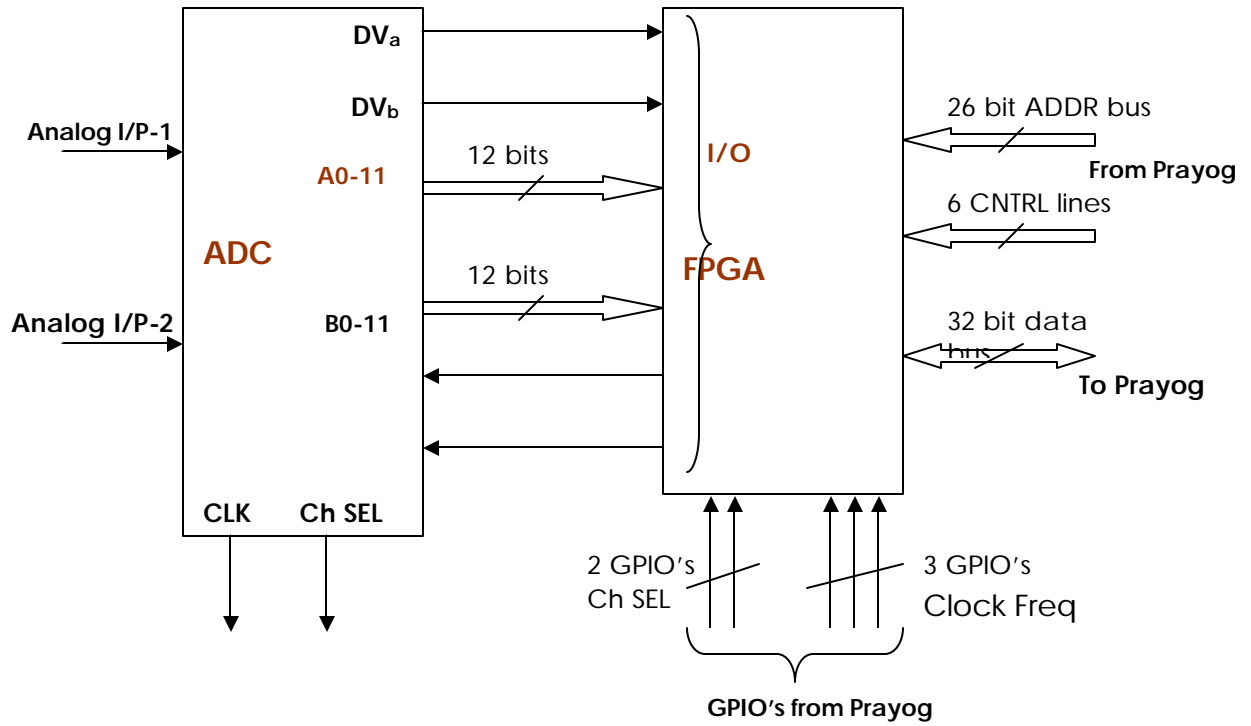
### **Aspire's Scope**

- Design of 12 bit ADC which can support up to at 50MCps and communicates with the host SA1110 based embedded Linux board on local bus
- Develop host driver software for channel selection and sampling rate of ADC
- Development of API on the PC side to initiate ADC card to capture data from the field and transfer the captured data from host memory to the PC

### **Proposed system:**

- An ADC card designed around
  - Analog Device's ADS2807 which is a dual channel 12 bit high speed ADC supporting upto 50 Msps
  - Xilinx FPGA which sits on host local bus and controls the ADC. The FPGA chosen for this design is XCV600E-6HQ240C. The ADC card has the programming interface to program the FPGA.
- Driver software running on the host to initiate the ADC and control its operation thru FPGA. The FPGA initiates data capture from the field based on the command from the remote PC.
- While on power on both channels are selected, two GPIOs are used to select the ADC channels. Three more GPIOs are used to select ADC clock to program sampling rate
- API running on the desktop gives user the flexibility to select channel, sampling rate and start/stop option thru a menu driven interface. The PC communicates with host thru Ethernet

The system block diagram is as shown in the next page



Host Prayog – a SA1110 ased Linux platform

ADC ADS2807-dual channel 12 bit ADC supporting 50Msps

FPGA XCV600E-6HQ240C from Xilinx